

Method of Driving Liquid Crystal Display Device

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention relates to a method of driving an active matrix liquid crystal display device of in-plane switching mode.

Related Background Art

10 Conventional liquid crystal display devices undesirably produce image sticking, in which, when leaving an unchanging image on a screen for a long period of time, a faint remnant of the image remains even after a new image has replaced it. A driving method used to overcome this
15 problem is offset correction to correct the grayscale dependence of voltage drop induced by a gate signal. Another driving method for reducing the image sticking and eliminating flicker in a twisted nematic (TN) liquid crystal display device is as follows. In a grayscale where
20 a source signal has a large amplitude, the voltage of a common signal and the center voltage of the source signal are set to such values as to compensate the voltage drop induced by a gate signal. In a grayscale where the source signal has a small amplitude, on the other hand, the center voltage of the source signal is set to a value higher than
25 the above center voltage of the source signal for

compensating the voltage drop induced by the gate signal. This method is disclosed in Japanese Unexamined Patent Application Publication No. 2001-337310, pp. 2 - 5, and illustrated in Fig. 8 - 9, for example.

5 However, if the driving method described in the above application is applied to a liquid crystal cell of in-plane switching (IPS) mode, it is unable to prevent the image sticking. The liquid crystal cell of the IPS mode has electrodes parallel to each other, which is different from
10 that of the TN mode having electrodes opposite to each other, and a residual DC voltage is more likely to be retained in the IPS mode than in the TN mode, causing the image sticking.

SUMMARY OF THE INVENTION

15 In view of the foregoing, it is an object of the present invention to provide a method of driving a liquid crystal display device capable of reducing image sticking in a liquid crystal display device of IPS mode, not by a conventional offset correction of setting an optimum value
20 of Vcom for preventing unequal DC components between a pixel electrode voltage and a common electrode voltage, but by setting an offset value for preventing residual vertical DC voltages and image sticking.

25 To these ends, according to one aspect of the present invention, there is provided a method of driving a liquid crystal display device of in-plane-switching (IPS) mode for

applying an electric field substantially parallel to a substrate surface, having a pair of substrates, a liquid crystal layer placed between the pair of substrates, a plurality of gate lines placed above one of the pair of substrates, a plurality of source lines placed to cross the gate lines with an insulative layer interposed therebetween, a switching element placed in a near proximity to a crossing point of the gate lines and the source lines, and a pixel electrode connected to the source lines through the switching element, to which a signal voltage required for image display is supplied by the source line through the switching element, the method including a step of setting an average value of the signal voltage in such a way that an average value of a positive polarity voltage and a negative polarity voltage of the pixel electrode varies with a grayscale to be displayed, and a step of inputting the average value of the signal voltage to the pixel electrode. This method is capable of minimizing image sticking in IPS liquid crystal display devices.

In the above method, the average value of the signal voltage may be an average of two values of grayscale reference voltages input to a source line drive circuit for generating the signal voltage from an external unit.

According to another aspect of the present invention, there is provided a liquid crystal display device of in-plane-switching (IPS) mode for applying an electric

field substantially parallel to a substrate surface, including a pair of substrates, a liquid crystal layer placed between the pair of substrates, a plurality of gate lines placed above one of the pair of substrates, a plurality of source lines placed to cross the gate lines with an insulative layer interposed therebetween, a switching element placed in a near proximity to a crossing point of the gate lines and the source lines, and a pixel electrode connected to the source lines through the switching element, to which a signal voltage required for image display is supplied by the source line through the switching element, wherein an average value of the signal voltage supplied by the source line is set in such a way that an average value of a positive polarity voltage and a negative polarity voltage of the pixel electrode varies with a grayscale to be displayed. This IPS liquid crystal display device is capable of minimizing image sticking.

In the above liquid crystal display device of in-plane-switching mode, the average value of the signal voltage may be an average of two values of grayscale reference voltages input to a source line drive circuit for generating the signal voltage from an external unit.

The above and other objects, features and advantages of the present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of

illustration only, and thus are not to be considered as limiting the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

5 Fig. 1A is a view showing a liquid crystal display device according to an embodiment of the present invention.

Fig. 1B is a cross sectional view of the liquid crystal display device in Fig. 1A.

10 Fig. 2 is a circuit diagram of a liquid crystal display device according to an embodiment of the present invention.

Fig. 3 is a view showing a signal waveform of a liquid crystal display device according to an embodiment of the present invention.

15 Fig. 4 is a view showing a relationship between a capacitance and a signal voltage amplitude in a liquid crystal display device according to an embodiment of the present invention.

Fig. 5 is a circuit diagram of a liquid crystal display device according to an embodiment of the present invention.

20 Fig. 6A is a sectional view of a major part of a liquid crystal display device of IPS mode.

Fig. 6B is a sectional view of a major part of a liquid crystal display device of TN mode.

25 Fig. 7A is a view showing a polarity inversion driving method in a liquid crystal display device according to an embodiment of the present invention.

Fig. 7B is a view showing a polarity inversion driving method in a liquid crystal display device according to an embodiment of the present invention.

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DESCRIPTION OF THE PREFERRED EMBODIMENTS

A transmissive liquid crystal display device applies an electric field to liquid crystal filled between two substrates and controls the alignment of liquid crystal molecules according to the strength of the electric field, thereby adjusting the amount of light passing through the substrate to produce an image with a desired brightness. In an active matrix liquid crystal display device with a switching element comprising a thin film transistor (TFT) and so on, in-plane switching (IPS) mode that applies an electric field parallel to a substrate to liquid crystal is used as a technique to obtain an extremely wide viewing angle. The IPS mode operation can minimize viewing-angle-based grayscale inversion and deterioration in contrast ratio.

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Referring first to Fig. 1A, a plan view of a pixel area of a standard IPS liquid crystal display device is shown. Fig. 1B is a sectional view thereof. The liquid crystal display device has a TFT array substrate 100 and a color filter substrate 200.

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The TFT array substrate 100 has a plurality of gate lines 1 placed on an insulative substrate 101, an insulative

layer 2 placed over the gate lines, a source line 3 placed to cross the plurality of gate lines 1, and an insulative layer 4 placed over the source line 3. The gate lines 1 and the source line 3 are connected to a switching element 5 such as TFT placed at their crossing point. A V-shaped comb-type pixel electrode 6 consisting of a plurality of electrodes placed parallel to the source line 3 is connected to the switching element 5. A V-shaped comb-type common electrode 7 also consists of a plurality of electrodes, placed parallel to and alternating with the plurality of electrodes of the pixel electrode 6. The pixel electrode 6 is formed by a metal such as chromium (Cr), aluminum (Al), and molybdenum (Mo), or a transparent conductive film such as Indium Tin Oxide (ITO). A storage capacitor line 8, formed by a metal such as chromium (Cr), aluminum (Al), and molybdenum (Mo), is connected to the common electrode 7 through a through-hole. The TFT array substrate 100 and the color filter substrate 200 are placed face to face and a liquid crystal layer 9 is interposed between, which makes up a liquid crystal panel 10. Further, a backlight and other components are set to the liquid crystal panel 10, thereby producing a liquid crystal display device. A voltage is applied to the liquid crystal layer 9 between the pixel electrode 6 and the common electrode 7, and an electric field substantially parallel to the substrate is thus applied to the liquid crystal layer 9.

In a standard liquid crystal display device of the
IPS mode, an active area of the liquid crystal is surrounded
by lamination of dielectric films, such as an alignment
layer (PI) 61, an protective layer (OC) 62, a color material
5 of a color filter (CF) 63, a glass material of an insulative
substrate 101, and so on, as shown in Fig. 6A. An electric
field E for driving the liquid crystal, created between the
pixel electrode 6 and the common electrode 7, extends into
the laminated films. In the liquid crystal display device
10 of the TN mode, on the other hand, the pixel electrode 6
and the common electrode 7 are placed face to face, and an
electric field E for driving the liquid crystal is created
only between the pixel electrode 6 and the common electrode
7, as shown in Fig. 6B. Hence, though the TN mode can avoid
15 image sticking by preventing DC component between the pixel
electrode 6 and the common electrode 7, the IPS mode cannot
eliminate the image sticking by the conventional offset
correction method due to a residual DC voltage left in the
dielectric lamination films.

20 Referring then to Fig. 2, a circuit diagram of a liquid
crystal display device of the IPS mode is shown. As shown
in Fig. 2, a plurality of the horizontal gate lines 1 and
a plurality of the vertical source lines 3 cross
perpendicularly. The area surrounded by the gate line 1
25 and the source line 3 is one pixel area. The switching
element 5 is placed near the crossing point of the two lines.

The pixel electrode 6 is connected to a drain electrode 23 and placed parallel to the common electrode 7. The source lines 3 are connected to a source line drive circuit 11 for signal voltage supply. The source line drive circuit 11 supplies a grayscale signal (signal voltage) in accordance with a pixel to be driven to the liquid crystal panel 10. A gate line drive circuit 12 supplies a gate voltage for turning on/off the switching element 5. A common voltage is supplied to the common electrode 7.

The circuit shown in Fig. 2 has capacitance C_{lc} with liquid crystal between the pixel electrode 6 and a counter electrode, capacitance C_{gd} between the gate and the drain, and storage capacitance C_{st} . The common electrode 7 is kept at a constant common voltage. On the other hand, a signal voltage 32 is written to the pixel electrode 6 from the switching element 5 through the drain electrode 23, thus controlling an electric field in the liquid crystal layer 9 and displaying images.

The operation of a voltage of pixel electrode (hereinafter as a pixel voltage 31) will be explained hereinafter with reference to Fig. 3 showing the waveforms of the voltages applied to the gate line 1 and the source line 3. In a standard liquid crystal display device, the relative polarity of the pixel voltage 31 to the common voltage 34 is inverted at every frame so as to avoid deterioration of liquid crystal. Thus, the polarity of the

pixel electrode 6 relative to the common voltage 34 is inverted at every frame, a time period in which all the gate lines 1 are selected sequentially.

If a positive pulse with a higher voltage than a threshold voltage of the switching element 5 is applied to the gate electrode 21, the switching element 5 turns on, that is, it turns to a high level, in which a source electrode 22 and the drain electrode 23 have electrical continuity. The signal voltage 32 on the source line 3 is thereby sent to the pixel electrode 6. The signal voltage 32 is an alternating voltage with the center voltage of V_{so} and the amplitude of V_{sa} . The amplitude V_{sa} is in accordance with the grayscale to be displayed. The pixel voltage 31 rises in synchronization with the gate voltage 33, as shown in Fig. 3. Upon switching the gate voltage 33 to a low level to turn off the switching element 5, feedthrough of ΔV_{gd} occurs in the pixel voltage 31 due to the capacitance C_{gd} between the gate and the drain. For one frame period after that, the pixel voltage 31 is retained by the storage capacitance C_{st} . The common voltage 34 is set so as to equalize the absolute value of a voltage V_1 applied to the liquid crystal in the first frame period and that of a voltage V_2 applied thereto in the second frame period, and the common voltage 34 of this value is called an optimum V_{com} . The common voltage 34 may be adjusted with a variable resistor in such a way that the absolute values of V_1 and

V2 are the same.

A voltage drop ΔV_{gd} of the pixel voltage 31 due to the feedthrough is expressed by:

5 Formula 1: $\Delta V_{gd} = \Delta V_g \times C_{gd} / (C_{lc} + C_{gd} + C_{st})$

where ΔV_g is a change in the gate voltage.

After the pixel voltage 31 is kept at a constant value for one frame period, in the second frame period, upon the gate voltage 33 turning again to the high level, the pixel voltage 31 turns to a level of the signal voltage 32 with reverse polarity to the previous (first) frame period.

10 Then, in synchronization with the gate voltage 33 turning back to the low level, the pixel voltage 31 drops as in the first frame period, and further drops by ΔV_{gd} due to the feedthrough.

15 Of the elements of Formula 1, C_{lc} is dependent on the signal voltage (grayscale voltage). The value of the capacitance C_{lc} with the liquid crystal thus varies according to the grayscale of image applied to the liquid crystal. C_{st} and C_{gd} have little voltage dependence.

20 Referring now to Fig. 4, a relationship between C_{lc} and amplitude V_{sa} of the signal voltage 32 is shown. As the signal voltage 32 increases, C_{lc} increases, and accordingly ΔV_{gd} decreases in inverse proportion to the signal voltage 32. Thus, ΔV_{gd} is not constant but varies 25 with the amplitude of the signal voltage 32, as expressed by Formula 1. Hence, in order to equalize the absolute

value of the voltage V1 applied in the first frame period
and that of the voltage V2 applied in the second frame period
in each grayscale, it is necessary to set the value of V_{so}
in accordance with changes in ΔV_{gd} . This is called the
5 offset correction. TN liquid crystal display devices
generally prevent the image sticking with this method.
Another method to prevent the image sticking is to set a
high value for V_{so} at the grayscale with small_V_{sa}, as
described above. This embodiment sets a value of V_{so} for
10 preventing the image sticking in the IPS liquid crystal
display device without using the above method of the V_{so}
setting.

A method of setting V_{so} will be explained below.
Referring to Figs. 2 and 3, a control circuit 13 controls
15 the output timing and the value of the gate voltage 33 output
from the gate line drive circuit 12, the signal voltage 32
output from the source line drive circuit 11, and the common
voltage 34 applied to the common electrode 7. For example,
with 256 levels of grayscale reproduction, a given value
20 of the signal voltage 32 selected from 256 levels, positive
and negative polarities each, of voltages is applied to the
pixel electrode so as to reproduce the grayscale. Thus,
it is necessary to output the signal voltages 32 of 256
25 different levels, positive and negative polarities each,
from the source line drive circuit 11.

Now, a unit of generating 256 levels of the signal

voltages 32 will be explained below. Referring to Fig. 5, it is an explanatory view showing an example of the source line drive circuit 11, a unit of generating 256 levels of the signal voltages. As shown in Fig. 5, there are provided
5 an input terminal 41 of the source line drive circuit 11 from a DC power source 14, an input terminal 42 of the source line drive circuit 11 from the control circuit 13, a divided resistor 43, and an output terminal 44 of the source line drive circuit 11. The input terminal 42 of the source line drive circuit 11 is connected to the control circuit 13 and control signals are input to the input terminal 42. The input terminal 41 of the source line drive circuit 11, on the other hand, is connected to the DC power source 14 and grayscale reference voltages of 16 different levels
10 (values) are input the input terminal 41. For example, 16 levels of grayscale reference voltages, which are, the first grayscale reference voltage (V_{ref0}), the second grayscale reference voltage (V_{ref1}), to the fifteenth grayscale reference voltage (V_{ref14}), and the sixteenth grayscale reference voltage (V_{ref15}), are applied,
15 respectively, to the input terminals 41 from output terminals of the DC power source 14. Divided resistors 43 connected in series are connected between the input terminals 41.
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25 For example, 15 divided resistors 43 are connected between the input terminal 41 with the first grayscale

reference voltage (V_{ref0}) and the input terminal 41 with the second grayscale reference voltage (V_{ref1}). From output terminals 45 placed at each connection of the divided resistors 43, 15 signal voltages of different levels, which are, the signal voltages indicating the first screen voltage (V_{s0}), the second screen voltage (V_{s1}) to the sixteenth screen voltage (V_{s15}), divided by the 15 divided resistors are respectively output. With the signal voltages between all V_{ref} , it is able to generate 256×2 levels of signal voltages; 256 levels at the positive polarity side and 256 levels at the negative polarity side. A given voltage is selected from those signal voltages in a selection circuit 46 and output to the liquid crystal panel 10 through the output terminal 44.

Table 1 shows the grayscale reference voltage V_{ref} input to the source line drive circuit 11, and the amplification V_{sa} and the center voltage V_{so} of the signal voltage 32 output from the source line drive voltage 11 according to this embodiment. For example, in the case of the grayscale of 255, the center voltage V_{so} of the signal voltage 32 input to the source line drive circuit 11 is 7.435V, which is the average of the grayscale reference voltages $V_{ref0} = 14.670V$ and $V_{ref15} = 0.200V$. In the grayscale of 0, V_{so} is 7.355V, the average of $V_{ref7} = 7.985V$ and $V_{ref8} = 6.725V$. These set values are determined by a test of examining the degree of image sticking with varying

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Vref. The set values may be adjusted according to the specifications of the liquid crystal display device. This method can prevent DC component from remaining in the dielectric lamination films, thereby minimizing the image sticking.

TABLE 1

GRAYSCALE	V _{s a}	V _{s o}	VOLTAGE VALUE
255	7.235	7.435	V _{ref 0} = 14.670
240	6.410	7.313	V _{ref 1} = 13.723
192	5.210	7.135	V _{ref 2} = 12.345
127	4.000	6.955	V _{ref 3} = 10.955
64	2.800	7.097	V _{ref 4} = 9.897
32	1.950	7.198	V _{ref 5} = 9.148
1	0.700	7.347	V _{ref 6} = 8.047
0	0.630	7.355	V _{ref 7} = 7.985
			V _{ref 8} = 6.725
			V _{ref 9} = 6.647
			V _{ref 10} = 5.248
			V _{ref 11} = 4.297
			V _{ref 12} = 2.955
			V _{ref 13} = 1.925
			V _{ref 14} = 0.903
			V _{ref 15} = 0.200

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This embodiment shows a case where the difference (V_{s o255}-V_{s o127}) between V_{s o} at the grayscale of 255 (V_{s o255}) and V_{s o} at the grayscale of 127 (V_{s o127}) is 480mV, and the difference (V_{s o0}-V_{s o127}) between the V_{s o} at the grayscale of 0 (V_{s o0}) and V_{s o127} is 400mV. In other cases, however, either or both of these values can be substantially 0mV or negative. These values may vary with the combination

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or the interface state of the alignment layer 61, the protective layer 62, and the material of the color filter 63.

In the liquid crystal display device according to this embodiment, as in standard liquid crystal display devices, adjustment of Vcom is performed with an intermediate grayscale image at the grayscale of 127, which is the intermediate value between the grayscales of 0 and 255. If the liquid crystal display device uses a dot-inversion driving method and so on, it displays a checkered pattern, for example, and adjusts the value of Vcom in such a way that the pixel area with minimum flicker has an optimum Vcom. Hence, though substantially no flicker occurs at the grayscale of 127, flicker is likely to occur at the other grayscales since their Vcom values are off the optimum Vcom value. The flicker of images can be prevented by dot-inversion driving that reverses the polarity from pixel to pixel as shown in Fig. 7A, 1×2 driving as shown in Fig. 7B, and driving that randomly reverses the polarity, which is not shown. In Figs. 7A and 7B, the symbol "+" indicates that a pixel voltage relative to a common voltage is positive, and the symbol "-", negative. Though the case of adjusting Vcom at the grayscale of 127 is shown here, the adjustment of Vcom may be performed at the other grayscales since it has the same effect.

As described above, the present invention provides

a method of driving a liquid crystal display device capable of minimizing image sticking in an IPS liquid crystal display device by setting an average value of the signal voltages in such a way that an average value of a positive polarity voltage and a negative polarity voltage of the signal voltages supplied to the pixel electrode varies with 5 grayscale.

From the invention thus described, it will be obvious that the embodiments of the invention may be varied in many 10 ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended for inclusion within the scope of the following claims.